UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/763,365	02/23/2001	Teruo Takizawa	108680	4673

25944 7590 09/25/2003

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
HOGANS, DAVID L	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/763,365	TAKIZAWA ET AL.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Amendment E filed on July 16, 2003.

Status of Claims

Claims 1-16 are cancelled. Claims 17-27 are pending. Claims 28-31 are new.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17-20, 22-26 and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 10027854 to Nagashima et al.

Claim 17

Nagashima et al. teaches a metal-oxide-semiconductor field-effect transistor including: a silicon substrate (10), a gate insulation film (23) on the silicon substrate (10), and a gate electrode (31 and 32) on the gate insulation film, the gate electrode including a germanium film (31) on the gate insulation film, wherein p-type impurities are doped into the germanium film (31) to form a film with a work function in the middle of N-type silicon and P-type silicon. (See machine translation and Figures 1-6) The Examiner notes that Nagashima et al. discloses identical reasons for p-type doping of a germanium film as does Applicant, for example: reduced threshold voltage for NMOS and PMOS, creation of surface channel CMOS with a single polar gate electrode and

reduction of the short channelization effect. (See machine translation paragraph [0009] and Applicant's own specification pages 13-15)

Nagashima et al. discloses the claimed invention except for wherein a range of concentration of the p-type impurities is about 10^{17} to 10^{20} cm^{-3}.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to optimize the p-type impurity concentration in the germanium layer, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e. – a p-type germanium film with a silicon mid range work function), discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955)

Claim 18

Incorporating all arguments of Claim 17 and noting that Nagashima et al. teaches wherein the germanium film includes at least one of a single-crystalline germanium film, a polycrystalline germanium film and an amorphous germanium film. (See machine translation and Figures 1-6)

Claim 19

Incorporating all arguments of Claim 17 and noting that Nagashima et al. teaches wherein the gate electrode includes a multi-layer structure having a low resistance conductive film. (See machine translation, notably paragraph [0020], and Figures 1-6)

Claim 20

Incorporating all arguments of Claim 19 and noting that Nagashima et al. teaches wherein the low resistance conductive film includes at least one of a transition metal, a transition metal silicide, and a transition metal nitride film. (See machine translation, notably paragraph [0020], and Figures 1-6)

Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select a preferred metal silicide, since it has been held to be within the general skill of a worker in the art to select a known material based on its suitability for its intended use. *In re Leshin*, 125 USPQ 416 (CCPA 1960)

Claims 22 and 23

Nagashima et al. teaches a metal-oxide-semiconductor field-effect transistor including: a silicon film/substrate (10), a gate insulation film (23) on the silicon film, and a gate electrode (31 and 32) on the gate insulation film, the gate electrode including a germanium film (31) on the gate insulation film, wherein p-type impurities are doped into the germanium film (31) to form a film with a work function in the middle of N-type silicon and P-type silicon. (See machine translation and Figures 1-6) The Examiner

notes that Nagashima et al. discloses identical reasons for p-type doping of a germanium film as does Applicant, for example: reduced threshold voltage for NMOS and PMOS, creation of surface channel CMOS with a single polar gate electrode and reduction of the short channelization effect. (See machine translation paragraph [0009] and Applicant's own specification pages 13-15)

Nagashima et al. discloses the claimed invention except for wherein a range of concentration of the p-type impurities is about 10^{17} to 10^{20} cm^{-3}.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to optimize the p-type impurity concentration in the germanium layer, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e. – a p-type germanium film with a silicon mid range work function), discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955)

Claim 24

Incorporating all arguments of Claim 22 and noting that Nagashima et al. teaches wherein the germanium film includes at least one of a single-crystalline germanium film, a polycrystalline germanium film and an amorphous germanium film. (See machine translation and Figures 1-6)

Claim 25

Incorporating all arguments of Claim 22 and noting that Nagashima et al. teaches wherein the gate electrode includes a multi-layer structure having a low resistance conductive film. (See machine translation, notably paragraph [0020], and Figures 1-6)

Claim 26

Incorporating all arguments of Claim 25 and noting that Nagashima et al. teaches wherein the low resistance conductive film includes at least one of a transition metal, a transition metal silicide, and a transition metal nitride film. (See machine translation, notably paragraph [0020], and Figures 1-6)

Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to select a preferred metal silicide, since it has been held to be within the general skill of a worker in the art to select a known material based on its suitability for its intended use. *In re Leshin*, 125 USPQ 416 (CCPA 1960)

Claims 28-29

Incorporating all arguments of Claim 17 and noting that Nagashima et al. teaches wherein the silicon substrate (10 and 12) is doped by boron p-type impurities. (See machine translation and Figures 1-6)

Claims 30-31

Incorporating all arguments of Claim 22 and noting that Nagashima et al. teaches wherein the silicon substrate (10 and 12) is doped by boron p-type impurities. (See machine translation and Figures 1-6)

3. Claims 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 10027854 to Nagashima et al. in view of Semiconductor Manufacturing Technology (2001) to Quirk et al.

Incorporating all arguments of Claims 17, 19, 22 and 25 and noting that Nagashima et al. fails to explicitly teach a wherein the multi-layer structure is provided with a polysilicon film in between the germanium film and the low resistance conductive film.

However, Quirk et al., on pages 309-311, teaches a polysilicon film that is covered with a refractory metal. Furthermore, Quirk et al. teaches that when the polysilicon and the refractory metal are alloyed together they form a silicide that exhibits low electrical resistivity (i.e. – polycides reduce the series resistance of an interconnection to a polysilicon gate) and are thermally stable.

It would have been obvious to one of ordinary skill in the art to modify Nagashima et al. by incorporating a polysilicon layer beneath the low resistance conductive film, as taught by Quirk et al., to provide a low electrical resistivity silicide contact to a gate.

Response to Arguments

3. Applicant's arguments with respect to claims 17-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

dh
September 9, 2003

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800